PATENT ABSTRACTS OF JAPAN

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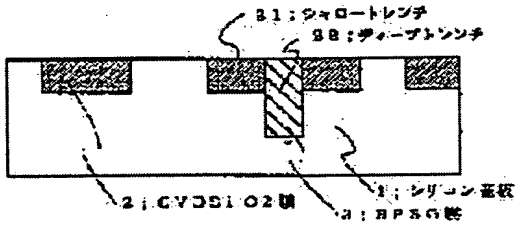
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To realize an element isolation structure composed of trenches different from each other in depth, a shallow trench and a deep trench provided inside the shallow trench, whereby a MOS transistor can be kept uniform in threshold voltage.
SOLUTION: An element isolation structure composed of trenches 21 and 22 different from each other in depth, a shallow trench 21 and a deep trench 22 provided inside the shallow trench 21, is provided to a silicon substrate 1, wherein a CVD SiO2 film 2 fills the shallow trench 21, and a BPSG film 3 fills the deep trench 22. As a MOS transistor is isolated by a shallow trench filled with an impurity-free SiO2 film, a diffusion layer is hardly formed near the shallow trench.



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